What is claimed is:

1. A semiconductor integrated circuit device comprising:

a first conductivity type semiconductor substrate connected to a first power supply;

a second conductivity type semiconductor layer provided on said first conductivity type semiconductor substrate or at a top surface of said first conductivity type semiconductor substrate and connected to a second power supply; and

a device forming portion provided on said second conductivity type semiconductor layer, with a decoupling capacitor formed at an interface between said first conductivity type semiconductor substrate and said second conductivity type semiconductor layer.

2. The semiconductor integrated circuit device according to claim 1, wherein said second conductivity type semiconductor layer is provided on an entire top surface of said first conductivity type semiconductor substrate or at said entire top surface of said first conductivity type semiconductor substrate, and a bottom surface of said first conductivity type semiconductor substrate is connected to said first power supply.

3. The semiconductor integrated circuit device according to claim 1, wherein said device forming portion has a first conductivity type well contacting said second conductivity type semiconductor layer and connected to a third power supply and another decoupling capacitor is

formed at an interface between said first conductivity type well and said second conductivity type semiconductor layer.

4. The semiconductor integrated circuit device according to claim 1, wherein said device forming portion has:

another second conductivity type semiconductor layer electrically connected to said second conductivity type semiconductor layer, and

a first conductivity type well provided on said another second conductivity type semiconductor layer contacted with said another second conductivity type semiconductor layer and connected to a third power supply, and

another decoupling capacitor is formed at an interface between said first conductivity type well and said another second conductivity type semiconductor layer.

5. The semiconductor integrated circuit device according to claim 3, wherein said device forming portion has an active element connected to said third power supply.

6. The semiconductor integrated circuit device according to claim 3, wherein a potential of said third power supply differs from potentials of said first and second power supplies.

7. The semiconductor integrated circuit device according to claim 1, wherein said first conductivity type semiconductor substrate has:

a substrate body, and

a surface portion having a lower resistivity than that

of said substrate body.

8. The semiconductor integrated circuit device according to claim 1, wherein said second conductivity type semiconductor layer is locally provided on said first conductivity type semiconductor substrate or at the top surface of said first conductivity type semiconductor substrate, said device forming portion is formed in that region in the top surface of said first conductivity type semiconductor substrate where said second conductivity type semiconductor layer is not provided, and said first conductivity type semiconductor substrate is connected to said first power supply via said device forming portion.

9. The semiconductor integrated circuit device according to claim 8, wherein said device forming portion has a first conductivity type well and said first conductivity type semiconductor substrate is connected to said first power supply via said first conductivity type well.

10. The semiconductor integrated circuit device according to claim 8, wherein said first conductivity type semiconductor substrate has:

a substrate body, and

a surface portion having a lower resistivity than that of said substrate body.

11. The semiconductor integrated circuit device according to claim 10, wherein said substrate body has a resistivity of 100 Ω·cm or higher.

12. The semiconductor integrated circuit device

according to claim 1, wherein said second conductivity type semiconductor layer is connected to said second power supply via said device forming portion.

13. The semiconductor integrated circuit device according to claim 12, wherein said device forming portion has a second conductivity type well and said second conductivity type semiconductor layer is connected to said second power supply via said second conductivity type well.

14. A semiconductor integrated circuit device comprising:

a first conductivity type semiconductor substrate connected to a first power supply; and

a device forming portion provided on said first conductivity type semiconductor substrate and having a second conductivity type well connected to a second power supply, with a decoupling capacitor formed at an interface between said first conductivity type semiconductor substrate and said second conductivity type well.

15. The semiconductor integrated circuit device according to claim 14, wherein said first conductivity type semiconductor substrate has:

a substrate body, and

a surface portion having a lower resistivity than that of said substrate body.

16. A semiconductor integrated circuit device comprising:

a substrate;

a first first conductivity type semiconductor layer

connected to a first power supply provided at least a part of said substrate;

a second conductivity type semiconductor layer provided on said first first conductivity type semiconductor layer and connected to a second power supply; and

a device forming portion provided on said second conductivity type semiconductor layer, with a decoupling capacitor formed at an interface between said first first conductivity type semiconductor layer and said second conductivity type semiconductor layer.

17. The semiconductor integrated circuit device according to claim 16, wherein said first first conductivity type semiconductor layer is provided selectively on said substrate, said device further comprises a second first conductivity type semiconductor layer, provided in that region where said first first conductivity type semiconductor layer and said second conductivity type semiconductor layer are not provided, connected to said first first conductivity type semiconductor layer and said first power supply, and said first first conductivity type semiconductor layer is connected to said first power supply via said second first conductivity type semiconductor layer and said device forming portion.

18. The semiconductor integrated circuit device according to claim 17, wherein said device forming portion has a first conductivity type well and said first first conductivity type semiconductor layer is connected to said first power supply via said second first conductivity type

semiconductor layer and said first conductivity type well.

19. The semiconductor integrated circuit device according to claim 17, further comprising a third first conductivity type semiconductor layer provided between said substrate and said first first conductivity type semiconductor layer and connected to said first first conductivity type semiconductor layer and said second first conductivity type semiconductor layer.

20. The semiconductor integrated circuit device according to claim 16, wherein said substrate has a resistivity of 100 Ω·cm or higher.

21. The semiconductor integrated circuit device according to claim 16, wherein said second conductivity type semiconductor layer is connected to said second power supply via said device forming portion.

22. The semiconductor integrated circuit device according to claim 21, wherein said device forming portion has a second conductivity type well and said second conductivity type semiconductor layer is connected to said second power supply via said second conductivity type well.

23. The semiconductor integrated circuit device according to claim 14, wherein said device forming portion has an active element connected to third and fourth power supplies, and a potential of said third power supply differs from potentials of said first and second power supplies.